Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A wafer level passive component, suitable for a chip, the chip at least having an active surface, a first contact pad, a second contact pad and a passivation layer, the first contact pad and the second contact pad disposed on the active surface, the passivation layer disposed on the active surface and exposing the first contact pad and the second contact pad, the wafer level passive component at least comprising:
a first conductive pattern, lying over the active surface and having a first connecting area and a first overlapping area, wherein the first connecting area connects to the first contact pad and the first overlapping area lies on the passivation layer;
a dielectric pattern, lying on the first overlapping area; and
a second conductive pattern, lying over the active surface and having a second connecting area and a second overlapping area, wherein the second connecting area connects to the second contact pad, the second overlapping area lies on the dielectric pattern, and at least a portion of the dielectric pattern is interposed between the first overlapping area and the second overlapping

area.

[c2] 2. The wafer level passive component of claim 1, wherein the first conductive pattern includes at least a metal layer.

[c3] 3. The wafer level passive component of claim 1, wherein the second conductive pattern includes at least a metal layer.

[c4] 4. The wafer level passive component of claim 1, wherein a material of the portion of the dielectric pattern is aluminum oxide.

[c5] 5. The wafer level passive component of claim 1, wherein the portion of the dielectric layer is made of a material with high dielectric constant.

[c6] 6. The wafer level passive component of claim 1, further comprising a dielectric layer covering a portion of the first conductive pattern.

[c7] 7. The wafer level passive component of claim 1, further comprising an under bump metallurgy layer interposed between the first conductive pattern and the first contact pad.